Thermo Electric Generator Material

Generating Electricity from Waste Heat

Thermoelectric generators (TEG) are based on the Seebeck effect, where a temperature difference is converted into electrical power making them attractive in diverse energy harvesting applications such as automobiles, waste heat recovery from industrial process, smart buildings, wireless sensing network (WSN) and Internet of Things (IoT) (Figs. 1a and 1b). Market survey showed a demand for "deploy & forget" solution that eliminates the battery replacement maintenance cycle for WSN and IoT applications. The employment of TEG to power the sensors instead of batteries is cost effective and therefore very promising. However, the TEG devices should be miniaturized to be integrated on the chip using a semiconductor fabrication compatible process that is facile, cost effective and industrially scalable. Our group at the Tyndall National Institute is involved in the research and development of TEG using electroplating technique that is Si-fab compatible process with an aim to bridge the gap between research and industrial production of efficient thermoelectric devices. The potential of a material for thermoelectric applications is evaluated by a dimensionless parameter called the figure of merit, *zT* and is defined as

$$zT = \frac{\alpha^2\sigma}{\kappa} T \qquad (1)$$

where, α is the Seebeck coefficient, σ is the electrical conductivity, κ is the total thermal conductivity, and T is the absolute temperature at which the properties are measured. For an efficient thermoelectric material zT should be as high as possible that is achieved by maximizing the power factor $\alpha^2\sigma$, while simultaneously minimizing κ. The Seebeck coefficient enters as a squared quantity in Eq. (1) and has a strong influence on zT.

Tellurium (Te) composition in bismuth telluride alloys plays a crucial role in determining the thermoelectric properties. Currently, Te content in thin films is maintained by annealing films in Te atmosphere for 60 hours. This makes the process cumbersome and expensive requiring sophisticated instrumentation to handle toxic element (Te) and incompatible with Si based fabrication process, thereby a hurdle in mass production of thermoelectric devices. We propose an innovative route of encapsulating thin Te layer between *p*-type SbBiTe alloy films to preserve tellurium stoichiometry in the electroplated thin films under annealing [1]. The encapsulation strategy increases Seebeck coefficient of annealed thin film with tellurium layer to about 175 μVK^{-1}, which is twice higher compared to films with no tellurium layer (Figs. 1c and 1d). Thus, tellurium encapsulation in thin films allows the process to be clean and environmental friendly without the need for sophisticated instrumentation to handle the toxic element. Inceptive wafer-scale processes were developed to construct thermoelectric devices on 4-inch Si wafers (see Fig. 2). BiTe alloy material electroplated as continuous thin film on a 4-inch wafer or on patterned 4-inch wafer as illustrated in Fig. 2. The optical micrographs of the substrate/die illustrate the pillars shape/dimensions along with the alignment marks used for flip-chip bonding (see Figs. 2c and 2d). We have also developed intellectual properties on the selective etching of bismuth telluride based materials without etching other materials on the wafer [2] that provides another route to fabricate these devices. TEG device on the chip is fabricated by flip-chip bonding of p-type substrate/tile with n-type tile/substrate (Fig. 2e)

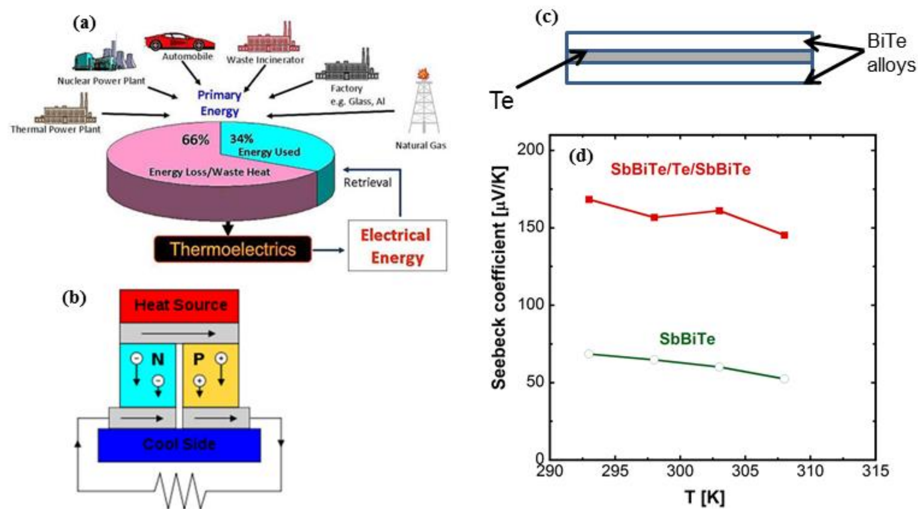

Fig. 1. (a) Waste heat produced in different applications that can be converted into usable electricity by thermoelectric power generator (taken from [3]), (b) Schematic sketch of a thermoelectric generator with p-and n-type materials that can convert waste heat into electricity, (c) Encapsulation concept in BiTe alloy material for enhanced thermoelectric properties, (d) Seebeck coefficient of $(Sb_{1-x}Bi_x)_2Te_3$ thin films with and without Te encapsulation.

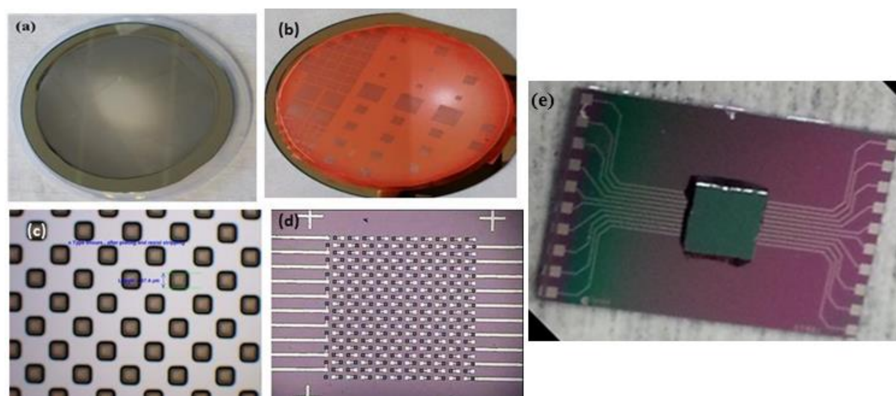

Fig. 2. Electrodeposited BiTe-alloy thin films on a 4-inch Si wafer: (a) Continuous film on seed layer, (b) Patterned film on seed layer with photoresist, (c) Optical image of the substrate/die after removing the photoresist depicting pillars dimensions and (d) Optical micrograph of the tile with individual pillars (p and n-type materials) along with the alignment marks for flip-chip bonding process. (e) TEG on the chip obtained by flip-chip bonding of p-type substrate/tile with n-type tile/substrate.

References

1. K. M. Razeeb and D. Gautam, *U.S. patent application Serial No.* US 15/291,782, 2016.
2. D. Gautam and K. M. Razeeb, "Anisotropic Wet Etching of Binary and Ternary Bi-Te Alloy System Compatible with Semiconductor Fabrication Process, under preparation, 2017.
3. http://www.sciencedaily.com/releases/2011/09/110920120238.htm